CLOCK AND DATA RECOVERY CIRCUIT AND CLOCK CONTROL METHOD

[0001]

FIELD OF THE INVENTION

This invention relates to a clock and data recovery method and a clock and data recovery circuit.

[0002]

BACKGROUND OF THE INVENTION

Fig.13 shows the structure of a conventional clock and data recovery circuit. From a reference clock (Ref CLK), multi-phase clocks (multiphase outputs), having an equally-spaced phase difference are generated by a voltage controlled oscillator (VCO) 51 of a phase locked loop(PLL). The VCO 51 is comprised of a ring oscillator of an analog circuit configuration, made up of an odd number of inverter circuits, connected in a ring topology. Multi-phase clocks with an equally spaced phase difference are output in a differential mode from differential inverter circuits of the respective stages making up the ring oscillator. An input data DATA is provided in common to data terminals of plural flip-flops 52 (F/F1 to F/F8) and respective multi-phase clock output from the VCO 51 are fed to clock terminals of the flip-flops 52 (F/F1 to F/F8) which sample the data DATA with rising or falling edges of clock signals and output the sampled data. The clock and data recovery circuit also includes a counter 53 which receives output data output from the plural flip-flops 52 (F/F1 to F/F8) to counts up and down logic values of the

output data, and a filter 55 which time-averages the output of the counter 53 over a preset time constant. An output voltage of the filter 55 is fed to the voltage-controlled oscillator (VCO) as its control voltage. Part or all of the outputs of the flip-flops 52 and one-phase clock output from the VCO 51 are output as data and clocks, respectively. The outputs of the plural flip-flops 52 (F/F1 to F/F8) are obtained on sampling the data DATA with clocks having phases shifted by a equal value and a sampling waveform which is equivalent to that of sampling the data with a frequency equal to eight times the frequency of the reference clock, is obtained, with the clock timing of a flip-flop, an output value of which does not coincide with the output value of the neighboring flip-flop representing a transition point of the data DATA.

[0003]

If a clock has a delay with respect to the data transition point, that is if the latch timing is delayed, the count value of the counter 53 is incremented to advance the clock phase, whereas, if the clock leads with respect to the data transition point, the count value of the counter 53 is decrement to delay the clock phase with respect to the data transition point. Meanwhile, the counter 53 may be made up of a charge pump (CP) which charges a capacitor with constant current when the output values of the plural flip-flops 52 (F/F1 to F/F8) are of logic 0 and discharges the capacitor with the constant current when output values of the plural flip-flops 52 (F/F1 to F/F8) are of logic 1.

[0004]

As a clock and data recovery circuit shown in Fig.13, reference may

be made to Publication 1 (ISSCC 1997 pp. 238 to 239 Alan Fiedler, "A. 1.0625GHz Tranceiver with 2x- Oversampling and Transmit Signal Preemphasis"). The clock and data recovery circuit, disclosed in the Publication 1, includes a receiver circuit which recovers clocks and data from serial input data to output the recovered clocks and data as parallel data. The VCO (voltage controlled oscillator) of the PLL (phase locked loop) includes a ring oscillator having ten delay stages (10-delay-stage), and 20 clock phases of the VCO provides 2x oversampling clocks to the receiver circuit recovering the clocks and data. The receiver circuit makes the VCO to be locked in input data to recover clocks from the transition of data of NRZ (non-return-to-zero) waveform. Meanwhile, in the clock and data recovery circuit, disclosed in the Publication 1, a data phase detector is made up of a plural number of high-speed latches, and an exclusive-OR logic gate for detecting coincidence/non-coincidence of the high-speed latches. The latch for sampling data bits is clocked with a positive-phase clock of the VCO, while the latch for sampling the boundary between data bits is clocked with a reverse-phase clock of the VCO.

[0005]

Fig.14 shows a schematic view of a structure of a clock control circuit, comprised of the combination of a DLL (delay synchronization loop) and an interpolator, as disclosed in Publication 2 (ISSCC 1997 p.p. 332 to 333, S. Sidiropoulos and Mark Horowitz et al., "A semi-digital delay locked loop with unlimited phase shift capability and 0.08-400 MHz operating range"). Referring to Fig.14, a DLL circuit 60 outputs multi-

phase clocks P1 to Pn, synchronized with an input clock. These multi-phase clocks P1 to Pn are fed to a switch 20. Two neighboring signals, selected by the switch 20, are fed to the interpolator (phase interpolator) 30. A signal corresponding to the interior division of the input two signals by the interpolator 30 is output at an output OUT. A control circuit 40 variably controls the interior division ratio of the interpolator 30, based on the result of detection of the phase difference between the output OUT and the reference clock, while controlling the switching of the switch 20.

[0006]

The interpolator 30 (phase interpolator) of Fig.14 is made up of an analog circuit shown in Fig.15. Referring to Fig.15, this phase interpolator includes N-channel MOS transistors MN61, and MN62, forming a first differential pair, the sources of which are connected in common to a first constant current source CS1, the gates of which receive differentially clocks IN1 and IN1B, outputs pair of which are connected to one end of a first load (a common drain of P-channel MOS transistors MP61 and MP62 connected in parallel) and to one end of a second load (a common drain of P-channel MOS transistors MP63 and MP64 connected in parallel). The phase interpolator also includes N-channel MOS transistors MN63, and MN64, forming a second differential pair, the sources of which are connected in common to a second constant current source CS2, the gates of which receive differentially clocks IN2 and IN2B, outputs pair of which are connected to one end of a first load (a common drain of P-channel MOS transistors MP61 and MP62 connected

in parallel) and to one end of a second load (a common drain of P-channel MOS transistors MP63 and MP64 connected in parallel). From the outputs pairs connected in common of the first and second differential pairs are output an output signals OUT and OUTB having the phases of the weighted sum of the two input clocks. In this phase interpolator, digital weight codes ictl (16 bits of b[0] to b[15]) are fed to first and second constant current sources CS1 and CS2 to vary the current values of the first and second constant current sources CS1 and CS2, for conversion to the phase of the output clock. That is, the number of the constant current source transistors $MN6B_1$ to $MN6B_{15}$ is selected by the turning on/off of the N-channel MOS transistors $MN6A_1$ to $MN6A_{15}$, the gate terminals of which receive 16 bits b[0] to b[15], respectively, to vary the current value.

[0007]

On the other hand, Publication 3 (ISSCC1999 p.p.180 to 181 "A2BParallel 1.25 Gb/s Interconnect I/O interface with Self Configurable Link and Plesiochronous Clocking") discloses a configuration, shown in Fig.16, as a phase interpolator. Referring to Fig.16, an output current of a current output type configuration which outputs an output current proportionate to the control circuit Ictl is mirrored by a first current mirror circuit (MN74, and MN75), and the mirrored current is received by a second current mirror circuit (MN73, and MN74), an output mirror current of which is fed to a differential pair circuit which receives as inputs the differential clock inputs IN, and INB. The differential pair circuit is provided with the current from the constant current source

transistor MN73 forming the second output end of the first current mirror circuit (MN74, and MN75) and clocks OUT, and OUTB, corresponding to phase shifted versions of the clocks IN, are output at the output nodes of the differential pair circuit. Meanwhile, the differential pair circuit includes N-channel MOS transistors MN71, and MN72, sources of which are connected in common to a constant current source transistor MP73 and the gates of which are fed with differential clock pairs IN, and INB, and P-channel MOS transistors MP71, and MP72, the sources of which are connected in common to the drain of an output transistor MP74 of the second current mirror circuit, the gates of which are fed with differential clocks IN, and INB and the drains of which are connected to the drains of the N-channel MOS transistors MN71, and MN72. Outputs OUT, and OUTB are taken at the drains of the of the N-channel MOS transistors MN71, and MN72. Across the drains of the N-channel MOS transistors MN71, and MN72 and the ground are connected capacitances C1, and C2, respectively, whereas, across the drains of the N-channel MOS transistors MN71, and MN72 are connected transistors N-channel MOS transistors MN76 and MN77 in series with each other. When the N-channel MOS transistors MN76 and MN77 are turned on, the outputs OUT, and OUTB are charged to an intermediate potential VDD.

[0008]

In Fig.16, when the clock IN makes a transition to a high level, the N-channel MOS transistor MN71 is turned on to turn the N-channel MOS transistor MN72 and the P-channel MOS transistor MN71 off and on, respectively to discharge the capacitor C1 while charging the capacitor

C2 with the outputs OUT and OUTB making transitions to a low and high level, respectively. When the clock IN makes a transition to a low level, the N-channel MOS transistor MN71 is turned off to turn the N-channel MOS transistor MN72 and the P-channel MOS transistor MP72 on and off, respectively to charge the capacitor C1, while discharging the capacitor C2, with the outputs OUT and OUTB making transitions to a high and low level, respectively. So, the clock frequency band is variably controlled by the control signal Ict1 supplied to the digital analog converter (DAC).

[0009]

As explained with reference to Figs.13 and 15, the above-described conventional circuit generates multi-phase clocks by the VCO circuit and, as an interpolator, a phase interpolator comprised of an analog circuit is adopted.

[0010]

Moreover, as shown in Fig.16, the analog phase interpolator has its band control being performed by the current which flows into the current source, such that, if a plural number of frequency bands are to be dealt with, such measures as widening the output current range of the constant current source is needed. In such case, it is not necessarily easy to compensate the linearity of the phase interpolator to enlarge the output current range of the constant current source.

[0011]

SUMMARY OF THE DISCLOSURE

It is therefore an object of the present invention to provide a clock and data recovery circuit and a clock control method, which facilitate

change of the frequency range and adjustment of characteristics.

It is another object of the present invention to provide a clock and data recovery circuit and a clock and a clock control method which make it possible to change the parallel number of data and clocks.

[0012]

For accomplishing the above object, a clock and data recovery circuit in accordance with one aspect of the present invention, comprises a plural number of latch circuits receiving an input data in common for sampling the input data with transition edges of clocks having phases shifted from one another, said clocks supplied respectively to said latch circuits, and for outputting the sampled data; a phase detection circuit for detecting a phase of a transition point of said input data associated with the clocks from outputs of said plural latch circuits and for outputting the detected phase; a filter for smoothing an output of said phase detection circuit; and a circuit for controlling the phase of said clocks based on an output of said filter. The clock and data recovery circuit recovering the clocks and data based on the input data;; wherein

a circuit for supplying the clocks with phases shifted from one another to said plural number of latch circuits includes:

a switch, receiving a plural number of clocks having respective different phases(referred to as multi-phase clocks), for selecting a plural number of sets of clock pairs from said multi-phase clocks; and

a plural number of interpolators, receiving plural sets of clock pairs, output from said switch, each interpolator outputting a signal the delay time of which is prescribed by the time corresponding to interior

division of the phase difference of said clock pair;

each of said interpolators including:

a circuit for turning a charging path and a discharging path of a capacitor on and off depending on logic values of input clock pairs; and

a buffer circuit for varying an output logic value when the magnitudes relation between the terminal voltage of said capacitor and a threshold value are inverted; the capacitance value of said capacitor being variably set by a control signal for determining the capacitance value; output signals of said plural interpolators being sent as clocks for said latch circuits; wherein

a circuit for controlling the phase of said clocks includes a decoder for decoding an output of said filter;

switching of selection of said clock pairs in said switch is controlled based on an output signal of said decoder, the interior division ratio of said plural interpolators being variably set and control being performed to advance or delay the phase of clocks supplied to said plural latch circuits.

In accordance with the present invention, each of said interpolators includes a logic circuit having first and second input terminals for receiving first and second input signals therefrom;

a switch inserted across a first power supply and an internal node and turned on when an output of said logic circuit is of a first logic value; and

a buffer circuit having its input terminal connected to said internal node and having an output logic value inverted on inversion of the

magnitudes relation between said internal node voltage and a threshold value;

there being also provided N pieces of second switches connected in parallel, each having one end connected to said internal node, and having a control terminal supplied with said first input signal from said first input terminal;

N pieces of third switches connected in parallel, each having one end connected to said internal node, and having a control terminal supplied with said second input signal from said second input end;

N pieces of fourth switches, connected in parallel across the other end of said second switch and a second power supply and each having a control terminal supplied with a control signal from said decoder so as to be turned on or off;

N pieces of fifth switches, connected in parallel across the other end of said third switch and the second power supply and each having a control terminal supplied with a control signal from said decoder so as to be turned on or off; and

a plural number of serial circuits inserted across said internal node and said second power supply and each being made up of a sixth switch and capacitor;

said sixth switch being turned on or off by a capacitance value determining control signal supplied to a control terminal of said sixth switch to variably control the value of the capacitance connected to said internal node.

In accordance with another aspect of the present invention, a clock

control method for a clock and data recovery circuit including a plural number of latch circuits receiving input data in common; said latch circuits sampling the input data with transition edges of clock signals having phases shifted from one another, said clock signals supplied respectively to said latch circuits to output the sampled data;

a phase detection circuit for detecting a phase of a transition point of said input data associated with the clocks from outputs of said plural latch circuits and for outputting the detected phase;

a filter for smoothing an output of said phase detection circuit; and

a circuit for controlling the phase of said clocks based on an output of said filter; said clock and data recovery method recovering the clocks and data based on the input data; comprising the steps of:

selecting by a switch receiving a plural number of clocks having respective different phases (termed multi-phase clocks), a plural number of sets of clock pairs from said multi-phase clocks and outputting the selected sets of the clock pairs;

with a plural number of interpolators receiving a plural number of sets of the clock pairs output form the switch, outputting a signal the delay time of which is prescribed by time corresponding to interior division of the phase difference of said paired clocks;

switching of selection of clock pairs in said switch being controlled based on an output signal of a decoder decoding the output of said filter; the interior division ratio of said interpolator being variably set to vary the phase of the clocks supplied to said plural latch circuits;

varying the capacitance value of each interpolator, having a circuit

for turning a charging path and a discharge path of a capacitor on and off, depending on the logic value of the input clock pair, and a buffer circuit for changing an output logic value when the magnitudes relation between the terminal voltage of said capacitor and the threshold value is changed, by a set of switches being turned on and off with capacitance determining control signals to enlarge the frequency range that can be coped with.

Still other objects and advantages of the present invention will become readily apparent to those skilled in this art from the following detailed description in conjunction with the accompanying drawings wherein only the preferred embodiments of the invention are shown and described, simply by way of illustration of the best mode contemplated of carrying out this invention. As will be realized, the invention is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects, all without departing from the invention. Accordingly, the drawing and description are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 shows a structure of an embodiment of the present invention.

Fig.2 shows the structure of a phase shift circuit according to an embodiment of the present invention.

Fig.3 shows the structure of a switch in a phase shift circuit of an embodiment of the present invention.

Fig.4 shows the structure of an interpolator in a phase shifting circuit according to an embodiment of the present invention.

Fig.5 is a timing waveform diagram for illustrating the operating

principle of the interpolator in a phase shifting circuit according to an embodiment of the present invention.

Fig.6 shows an illustrative structure of an interpolator in a phase shifting circuit according to an embodiment of the present invention.

Fig.7 shows an illustrative structure in case of employing an output of a multi-phase clock generating circuit as an input of the phase shifting circuit in an embodiment of the present invention.

Fig.8 shows a structure of a multi-phase clock generating circuit according to an embodiment of the present invention.

Fig.9 shows an illustrative structure of a four-phase clock generating circuit according to an embodiment of the present invention.

Fig.10 shows the timing operation of a four-phase clock multiplexer circuit according to an embodiment of the present invention.

Fig.11 illustrates the operation of an interpolator of a four-phase clock multiplexer circuit according to an embodiment of the present invention.

Fig.12 shows an illustrative structure of an interpolator of a four-phase clock multiplexer circuit according to an embodiment of the present invention.

Fig.13 shows an illustrative structure of a conventional clock and data recovery circuit. Fig.14 shows a structure of a conventional clock control circuit.

Fig.15 shows a structure of a conventional phase interpolator.

Fig.16 shows a structure of a conventional phase interpolator.

digital analog converter (DAC) constant current source transistor MP73

clock and data recovery circuit N-channel MOS transistors MN61, MN62.

[0013]

PREFERRED EMBODIMENTS OF THE INVENTION

Reference is made to the drawings for illustrating the embodiment of the present invention. A clock and data recovery circuit in accordance with the preferred embodiment of the present invention, shown in Figs.1 and 2, includes a phase shift circuit 10 which comprises a switch 110 for receiving plural clocks of respective different phases and outputting selectively a plural number of sets of paired clocks, and an interpolator 111 comprised of a plural number of interpolators 111 (INT1 to INT8), for receiving paired clocks output from the switch 110 and outputting output clocks the delay time of which is prescribed by the time obtained on dividing with a preset interior division ratio of the phase difference between the clock pairs. A clock and data recovery circuit in accordance with the preferred embodiment of the present invention further includes a plural number of latch circuits 102 (F/F1 to F/F8) for sampling input data with a rising edge or a falling edge of the clocks (CLK1 to CLK8) output from the plural interpolators, a counter 103 for up-counting or down-counting depending on whether the outputs of the plural latch circuits (F/F1 to F/F8) indicate up or down-counting, respectively, a filter 105 for time averaging the output of the counter 103 and a decoder 106 for decoding an output of the filter 105. The outline of the configuration and operation of the respective components are hereinafter explained.

[0014]

The interpolator 111 (INT1 to INT8) includes a circuit for turning a charging path and a discharge path of a capacitor on or off depending on the value of the input clock pairs (CMOS type inverters INV1 and INV2, the delay of which is changed, as shown in Fig.4), and a buffer circuit (INV3 of Fig.4), for varying the output logic value when the magnitude relation between the capacitor terminal voltage and a threshold value is inverted. The interpolator 111 is configured for variably setting the phase of the output signal, and for variably setting the capacitance values of the capacitor by a set of switches (MNA1 to MNA8 of Fig.4) on/off controlled by control signals for determining the capacitance value (Cnt of Fig.4[0:7]), in order to cope with a wide frequency range.

[0015]

The counter 103 may be constructed by a charge pump for turning the charging path on to charge the capacitor or turning the discharge path on to discharge the charge stored in the capacitor (equivalently adding or subtracting the stored charges) depending on the outputs of plural latch circuits (F/F1 to F/F8) 102. Alternatively, the counter 103 may be comprised of an up/down counter or an adder in a digital circuit configuration. The filter 105 is made up of a low pass filter of an analog circuit or a digital filter (averaging filter).

[0016]

Based on a switching signal U, output from the decoder 106, the combinations of the paired clocks in the switch 110 are switched. Moreover, based on the control signal S output from the decoder 106, the interior division ratios of the plural interpolators are variably controlled

to variably control the phase of the clock output from the plural interpolators 111.

[0017]

In an embodiment of the present invention, sets of output data of the plural latch circuits 102 (flip-flops F/F1 to F/F8) and clocks, such as, for example, a first-phase clock, output from the phase shift circuit 101, are entered to a selector 104, from which an optional set is selectively output. The number of data and clocks output in paral1el is rendered variable.

[0018]

For further explaining the above-described embodiment of the present invention in detail, a preferred embodiment of the present invention is now explained. Fig.1a shows the structure of an embodiment of the present invention. Referring to Fig.1a, a clock and data recovery circuit in accordance with one embodiment of the present invention includes a phase shift circuit 101, which receives eight-phase clocks and is adapted for outputting eight sets of clocks having phases being shifted, a plural number of D-type flip-flops 102 (F/F1 to F/F8), which receive at clock input terminals thereof the clock signal output from a phase shift circuit 101, receive an input data DATA at data input terminals thereof and are adapted for sampling the input data DATA with the rising edge of the clock, a counter 103 for upcounting and downcounting a count value in case of the output of the plural D-type flip-flops 102 being at logic 0 or at logic 1, respectively, a filter 105 for time averaging the output of the counter 103, a decoder 106 for decoding the output of the

filter 105, and a selector (selection circuit) 104 receiving one-phase clock output from phase shift circuit 101 and output data of the plural D-type flip-flops 102 (F/F1 to F/F8) to output selected sets (one-phase clock and sampled output data) in parallel based on the selection control signal. In Fig.1a, the selector 104 receives outputs of D-type flip-flops F/F1, F/F3, F/F5 and F/F7 as inputs among the plural D-type flip-flops (F/F1 to F/F8). Alternatively, outputs of all D-type flip-flops F/F1 to F/F8 may be fed to the selector 104.

[0019]

The D-type flip-flops 102 (F/F1 to F/F8) sample the input data DATA with the rising (or falling) edge of the clocks CLK1 to CLK8 output from the phase shift circuit 101 (see Fig.1b). From an output of the plural D-type flip-flops 102 (F/F1 to F/F8), such as "00001111", there is obtained waveform data on sampling the input data at a sampling period corresponding to one-eighth of the clock period. The input data undergoes a transition at a change point of output values of neighboring D-type flip-flops 102. The counter 103 counts outputs of the plural D-type flip-flops 102 and the resulting count values are smoothed by the filter 105 at a preset time constant to manage control as to whether or not the phase of clocks supplied to the plural D-type flip-flops is to be advanced or delayed, and hence clocks and data locked to the input data DATA are output.

[0020]

Fig.2 shows the structure of a phase shift circuit 101 in accordance with an embodiment of the present invention. Referring to Fig.2, the

phase shift circuit 101 includes a switch 110 fed with eight-phase clocks (8-phase CLK) and eight interpolators 111 (INT1 to INT8) fed with clock pairs output from the switch 110. The switch 110 is configured e.g., as a rotary switch and switches the combinations of output clock pairs based on outputs of the decoder circuit 106.

[0021]

Fig.3 shows an illustrative structure of the switch 110 (rotary switch) and the interpolator 111. Referring to Fig.3, this rotary switch includes a first switch 110-1 fed with odd-phased clocks (P0, P2, P4 and P6) of the eight-phased clocks P0 to P7 to output clocks selectively to the interpolator 111, and a second switch 110-2 fed with even-phased clocks (P1, P3, P5 and P7) of the eight-phased clocks P0 to Pn to output clocks selectively to the interpolator 111. In the initial state, in which switching control by the decoder 106 is not made, clock pairs (P0, P1), (P1, P2), (P2, P3), (P3, P4), (P4, P5), (P5, P6), (P6, P7), and (P7, P0), output by the first switch 110-1 and the second switch 110-2, are input to the interpolators 111_1 to 111_8.

[0022]

The decoder 106 provides control signals S, SB to the respective interpolators 111_1 to 111_8. If, when the interior division ratio (interior division ratio is w: 1-w in Fig.4 as later explained) of the phase difference of the interpolators 111_1 to 111_8 has reached upper or lower limit values, it is necessary to advance or delay further the phase, a switching signal U for switching the combinations of the clock pairs supplied to the interpolators 111_1 to 111_8 is output to the switches 110-1

and 110-2. For example, if the clock pair combinations (P0, P1), (P1, P2), (P2, P3), (P3, P4), (P4, P5), (P5, P6), (P6, P7), and (P7, P0) are fed to the interpolators 111_1 to 111_8, the clock pair combinations are switched to delay the clock phase, the clock pair combinations are switched to provide the combination of (P1, P2), (P2, P3), (P3, P4), (P4, P5), (P5, P6), (P6, P7), (P7, P0), and (P0, P1). The switch 110 is termed a rotary switch because it circulates or rotates the clock pair combinations.

[0023]

Fig.4 shows the circuit configuration of the interpolator 111 shown in Fig.2. Fig.5 shows the operation of the interpolator of Fig.4. Referring to Figs.4 and 5, the interpolator generates an output OUT having a delay time prescribed by the time obtained with interior division by w: 1-w of an interval between an output signal OUT1 having a delay time when the input signal IN1 is entered to the two inputs and an output signal OUT2 having a delay time when the input IN2 is entered to the two inputs. The interpolator includes CMOS inverters INV1, and INV2, receiving the inputs IN1, IN2 respectively and having the delay time being varied, an inverter 3, an input of which is connected to a common connection node(node N1) of the output of the inverters INV1, and INV2, and N-channel MOS transistors MNA1 to MNA8 and capacitors C0 to C7 connected in series between the node N1 and the ground. The N-channel MOS transistors MNA1 to MNA8 are turned on or off by the control signal Cnt[0:7] fed to the gates of the N-channel MOS transistors MNA1 to MNA8 to determine the value of the capacitance annexed to the node N1. Meanwhile, the capacitance values of the capacitances C0 to C7 may be

set to values corresponding to powers of 2, such as twice, four times, eight times and 16 times, with the C0 as reference. In this case, the W/L ratio (or gate width) of the N-channel MOS transistors MNA1 to MNA8 has such a size that conforms to the capacitance value of the corresponding capacitance.

[0024]

The control signal Cnt[0:7] may be set by an output of a frequency detection circuit which detects the frequency of the clock signal. Alternatively, the control signal Cnt[0:7] may be determined y setting the resistor or the dip switches to a desired value depending on the application. The frequency range that can be coped with may be enlarged by varying the capacitance value appended to the node N1 by the control signal Cnt[0:7].

[0025]

Fig.6 shows an schematic structure drawn at a transistor level of the interpolator 111 shown in Fig.2. Referring to Fig.6, the interpolator includes a P-channel MOS transistor MP51 which is connected across the power supply VDD and an internal node N51 and is turned on when an output signal from an logic OR circuit OR51 receiving the inputs IN1 and IN2 is at a low level. A plural number of series circuits of N-channel MOS transistors and capacitors (MN51- C1, ···, MN58- C8) are connected across the internal node N51 and the ground, whilst an inverter INV51 has an internal node N51 connected to an input terminal and has an output terminal from which an output signal OUT is output. The control signal Cnt[0:7], which are connected to the gates of the N-channel MOS

transistors MN51 to MN58, may be set by an output of the frequency detection circuit, not shown, adapted for detecting the frequency of the clock signal, or may be determined by setting e.g., registers or dip switches to desired values depending on applications. By varying the capacitance values connected to the node N51 by the control signal Cnt[0:7], it is possible to enlarge the frequency range that can be coped with.

[0026]

The interpolator also includes 2N pieces of N-channel MOS transistors MN11 to MN1N and MN21 to MN2N, the drains of which are connected to the internal node N51 and which are connected in parallel with one another, and 2N pieces of N-channel MOS transistors MN31 to MN3N andMN41 to MN4N, the drains of which are connected to the sources of the 2N N-channel MOS transistors MN11 to MN1N and MN21 to MN2N and the sources of which are connected to the ground. The gates of one half N of the 2N N-channel MOS transistors MN11 to MN1N are connected to the input signal IN1, in common, while the gates of the remaining half N of the 2N N-channel MOS transistors MN11 to MN1N are connected, in common, with the input signal IN2.

[0027]

By the control signal (N bits control code) S[0] to S[N-1] and the control signal (N bits control code) SB[0] to SB[N-1], input to the gates of the N-channel MOS transistors MN31 to MN3N and MN41 to MN4N, a preset number of the N-channel MOS transistors MN31 to MN3N and MN41 to MN4N are turned on. The N-bits control signal S[0:N-1] and

SB[0: N-1] are provided from the decoder 106, while SB[0] to SB[N-1] are given as complementary signals obtained on inverting S[0] to S[N-1] by the inverters(as shown by an inverter INV of Fig.3).

[0028]

Referring to Fig.6, the operation of the present interpolator is explained. When the inputs IN1, IN2 are both at a low level, the P-channel MOS transistor MP51, which receives at its gate an output of the OR circuit 51 is turned on to charge the capacitor C with the current from the power supply. The capacitance value of the capacitor C is the sum of the capacitance values of the capacitors which are connected to the N-channel MOS transistors MN51 to MN58 and which are set ON by the control signal Cnt among the capacitor C1 to C8.

[0029]

At the time of a rise transition from a low level to a high level of the signal applied to the input IN1, the N-channel MOS transistors MN11 to MN1N are turned on. Through a path of n pieces of N-channel MOS transistors, which are turned on by the control signal, among the N-channel MOS transistors MN31 to MN3N, the drains, sources and gates of which are connected to the sources of the N-channel MOS transistors MN11 to MN1N, to the ground and to the control signals S[0] to S[N-1], respectively, the charge stored in the capacitor C is partially discharged.

[0031]

At the time of a rise transition from a low level to a high level of t the input IN2, with a delay from the rise transition of the input IN1, the N-channel MOS transistors MN21 to MN2N are turned on. Through a

path of N-n pieces of N-channel MOS transistors, which are turned on by the control signal, among the N-channel MOS transistors MN41 to MN4N, the drains, sources and gates of which are connected to the sources of the N-channel MOS transistors MN11 to MnlN, to the ground and to the control signals SB[0] to SB[N-1], respectively, the charge stored in the capacitor C is partially discharged.

[0031]

The electric charge to be discharged until the output of the inverter INV51 receiving the terminal voltage of the capacitor C is inverted to a high level is assumed to be CV. The electric charge is discharged with the current nI during the phase difference T as from a transition of the input IN1 to a high level. The input IN2 then goes to a high level. The electric charge then is discharged with the drain current NI of n N-channel MOS transistors MN11 to MN1n and (N-n) N-channel MOS transistors MN21 to MN2(N- n), i.e., total N pieces of N-channel MOS transistors. The time delay from the rise of the input IN2 from the low level to the high level to the rise of the output OUT is given as

$$(CV-n \cdot I \cdot T)/NI$$
$$=CV/NI-n \cdot T/N \quad \cdots (1)$$

The delay time can be variably set with a unit of the N division of the phase difference T between the inputs IN1 and IN2.

In Fig.6, N-channel MOS transistors MN11 to MN1N and MN21 to MN2N, and 2N N-channel MOS transistors MN31 to MN3N and MN41 to MN4N may be arranged in the reverse positions. For example, drains of N-channel MOS transistors MN31 to MN3N and MN41 to MN4 are

connected to the internal node N51 and drains of N-channel MOS transistors MN11 to MN1N and MN21 to MN2N, sources of which are connected to the ground, are connected respectively to sources of N-channel MOS transistors MN31 to MN3N and MN41 to MN4.

[0032]

According to the present invention, the multi-phase clocks may be generated from a voltage-controlled oscillator (VCO) of the PLL. In this case, clocks are taken from the inversion circuit of a preset stage of the ring oscillator of the VCO. Alternatively, a multi-phase clock multiplier circuit may generate the multi-phase clocks.

[0033]

Fig.7 shows a configuration for generating the multi-phase clocks, supplied to the phase shift circuit 101, using a multi-phase clock generating circuit 200 employing a multiplier interpolator (multi-phase clock multiplier circuit). The phase shift circuit 101 of Fig.1 is made up of a multi-phase clock generating circuit 200 and a rotary switch 110. The interpolators 111_1 to 111_n output clocks CLK1 to CLKn, where n = 8, these clocks being fed to the clock input terminals of the D-flip-flop 102 of Fig.1 (F/F1 to F/F8). In Fig.7, reference clock generated by a clock generating circuit, such as a quartz oscillator, is used as a clock 1.

[0034]

Fig.8 shows an specified example of the structure of a four-phase clock multiplier circuit for generating four-phase clocks, as an example of the structure of the multi-phase clock generating circuit 200. Referring to Fig.8, this four-phase clock multiplier circuit includes a 1/4

frequency divider 201 for frequency dividing the input clock 205 by four to output four-phase clocks Q1 to Q4, n-stage cascaded four-phase clock multiplier circuits (termed also multiphase frequency doublers or MPFDs) 202_1 to 202_n and a period detection circuit 204. The last stage four-phase clock multiplier circuit 202_n outputs 2n-multiplied four-phase clocks Qn1 to Qn4. Meanwhile, the number of stages of the four-phase clock multiplier circuits is arbitrary. In this four-phase clock multiplier circuit, the four-phase clocks are rendered into eight phase by respective four-phase clock multiplier circuits 202 and are restored to the four phase to effect continuous multiplication. The eight-phase clocks (P21 to P28 of Fig.10) generated by the last stage four-phase clock multiplier circuit 202_n may also be directly output, as will now be explained in detail.

[0035]

Fig.9 shows an illustrative structure of the four-phase clock multiplier circuit 202_n when the multi-phase clock multiplier circuit is arranged as the four-phase clock multiplier circuit. The four-phase clock multiplexer circuits 202_1 to 202_n are of the same structure.

[0036]

Referring to Fig.9a, the four-phase clock multiplier circuit 202_n is made up of eight sets of timing difference division circuits 208 to 215, eight sets of pulse correction circuits 216 to 223 and four sets of multiplexer circuits 224 to 227. The timing difference division circuits 208 to 215 receive 4 phase clocks(Q(n-1)1- Q(n-1)4), divide the timing difference of two inputs, and output 8-phase output clocks. The odd number timing difference division circuits 208, 210, 212 and 214 receive

as two inputs, with the same clocks of the n-phase clocks (Q(n-1)1 and Q(n-1)1, Q(n-1)2 and Q(n-1)2, Q(n-1)3 and Q(n-1)3, Q(n-1)4 and Q(n-1)4), with the even number timing difference division circuits 209, 211, 213 and 215 receive neighboring clock pairs of the n-phase clocks (Q(n-1)1 and Q(n-1)2, Q(n-1)2 and Q(n-1)3, Q(n-1)3 and Q(n-1)4, Q(n-1)4 and Q(n-1)1).

[0037]

The number J pulse correction circuit, where $1 \leqq J \leqq 8$, receives an output of the number J timing difference division circuit as a first input, and an output of the number ((J+2) mod n) timing difference division circuit, where (J+2) mod n is the remainder obtained on dividing (J+2) by n, as a second input, while the number K multiplexer circuit, where $1 \leqq K \leqq 4$, receives an output of the number K pulse correction circuit and an output of the number (K+n) pulse correction circuit as an inputs. Fig.9b shows the structure of the pulse correction circuit and the pulse correction circuit is made up of a NAND circuit receiving a signal which is obtained on inverting the second input T23 by the inverter INV and with the first input T21 as inputs. Fig.9c shows the structure of a multiplexer circuit comprised of a two-input NAND circuit.

[0038]

Fig.10 is a signal waveform diagram showing the timing operation of the four-phase clock multiplier circuit 202 shown in Fig.9. The rising of a clock T21 is determined by the internal delay of the timing difference division circuit 208 as from the rising of the clock Q(n-1)1, the rising of a clock T22 is determined by the timing division of the timings of the rise

of the clock Q(n-1)1 and the rise of the clock Q(n-1)2 by the timing difference division circuit 209 and by the internal delay, and the rising of a clock T23 is determined by the timing division of the timings of the rise of the clock Q(n-1)1 and the rise of the clock Q(n-1)2 by the timing difference division circuit 210 and by the internal delay. In similar manner, the rising of a clock T26 is determined by the timing division of the timings of the rise of the clock Q(n-1)3 and the rise of the clock (n-1)4 by the timing difference division circuit 213 and by the internal delay, the rising timing of a clock T27 is determined by the internal delay of the timing of the rise of the clock Q(n-1)4 in the timing difference division circuit 214 and the rising of a clock T28 is determined by the timing division of the timings of the rise of the clock Q(n-1)4 and the rise of the clock (n-1)1 by the timing difference division circuit 215 and by the internal delay.

[0039]

The clocks T21 and T23, output by the timing difference division circuits 208, and 210, are input to the pulse correction circuit 216, which then outputs a pulse P21 having a falling edge determined by the clock T21 and a rising edge determined by the clock T23. In a similar sequence, pulses P22 to P28 are generated which are eight-phase pulses group, each of which has a duty of 25%, and has a phase shifted by 45° relative to one another. The clock P25, having a phase shifted by 180° relative to this clock P21, is multiplexed and inverted by a multiplexer circuit 224 and output as a 25 duty% clock Qn1. The clocks Qn1 to Qn4 are generated in similar manner. The clocks Qn1 to Qn4 are 50 duty%

four-phase pulse set of pulses, out of phase by 90° from one another. The period of the clocks Qn1 to Qn4 is doubled in frequency in the process of generating the clocks Qn1 to Qn4 from the clocks Q(n-1) to Q(n-1)4.

[0040]

That is, the eight-phase clocks P21 to P28 are generated from the four-phase clocks Q(n-1) to Q(n-1)4 to generate double-frequency four-phase clocks Qn1 to Qn4. Meanwhile, the eight-phase clocks P21 to P28 may be output from the last stage four-phase clock multiplexer circuit 202_n (see Fig.8).

[0041]

Fig.11 schematically shows the operating principle of the timing difference division circuits 208, and 209. The timing difference division circuits 208, 210, 212 and 214 (homo), receiving the same signals, output signals with an inherent delay time, whereas the timing difference division circuits 209, 211, 213 and 215 (hetero), receiving two inputs exhibiting the phase difference T, output signals which undergo transition with a delay time corresponding to the sum of the delay time proper to the timing difference division circuit and time T/2 corresponding to one half the phase difference T (halved phase difference T).

[0042]

Fig.12 shows a typical structure of the timing difference division circuits 208, and 209. The timing difference division circuit 208 has its two inputs IN1 and IN2 supplied with the same signals, whilst the timing difference division circuit 209 is supplied with two neighboring signals.

That is, the timing difference division circuit 208 has its two inputs IN1, and IN2 supplied with the same signals Q(n-1)1, whilst the timing difference division circuit 209 has its two inputs IN1 and IN2 supplied with Q(n-1)1 and Q(n-1)2. The structure of the timing difference division circuits, shown in Fig.12, comprises a P-channel MOS transistor MP01, having its source and drain connected to a power supply VDD and to the internal node N1, an OR circuit OR1, receiving the input signals IN1 and IN2 and having its output connected to the gate of the P-channel MOS transistor MP01 and N-channel MOS transistors MN01 and MN01, having drains connected to an internal node N1, sources connected to the ground via constant current source I0 and gates supplied with input signals IN1 and IN2. The internal node N1 is connected to an input terminal of the inverter INV01. The structure of the timing difference division circuits, shown in Fig.12, also includes, across the internal node N1 and the ground, are connected in parallel, a circuit made up of an N-channel MOS transistor MN11 and a capacitor CAP11 serially connected, a circuit made up of an N-channel MOS transistor MN12 and a capacitor CAP12 serially connected, ··· and a circuit made up of an N-channel MOS transistor MN15 and a capacitor C5P12 serially connected. The gates of the N-channel MOS transistors MN11, MN12, ··· and MN15 are supplied with a control signal 206 of a 5-bits width from the period detection circuit 204 designed for detecting the period of the input clock for turning the N-channel MOS transistors on and off. The size ratio of the gate width of the N-channel MOS transistors MN11 to MN15 and the capacitance of the capacitor CAP11 to CAP15 is set to, for example,

16:8:4:2:1, so that, based on the control signal 206 output from the period detection circuit 204 (Fig.8), the load connected to the common node can be adjusted to 32 steps to set the clock period.

[0043]

As for the timing difference division circuit 208, the charge at the node N1 is discharged through the two N-channel MOS transistors MN11 and MN12 by the rising edge of the clock Q(n-1)1, commonly supplied to the two inputs IN1 and IN2 thereof. When the electric potential of the node N1 reaches the threshold voltage of the inverter INV01, the clock T21, output by the node N1, rises. If the charge at the node N1, that need to be extracted until the threshold value of the inverter INV01 is reached, is CV, where C and V denote the capacitance and the voltage, respectively, and the discharge current by the N-channel MOS transistor is I, the charge CV is discharged with a constant current of 2I as from the rising of the clock Q(n-1)1. So, the time CV/2I represents the timing difference from the rising edge of the clock Q(n-1)1 until the rising of the clock T21 (propagation delay time).

[0044]

When the clock Q(n-1)1 is at a low level, the P-channel MOS transistor MP01 is turned on, the node N1 is charged to a high level and the output clock T21 of the inverter INV01 goes to a low level.

[0045]

As for the timing difference division circuit 209, charge at node N1 is extracted during the time after time tCKn (= multi-phase clock period) as from the rising edge of the clock Q(n-1)1. When the potential of the

node N1 has reached the threshold voltage of the inverter INV01, as from the rising edge of the clock Q(n-1)2 after time tCKn, the edge of the clock T22 rises. If the charge at the node N1 are CV and the discharge current of the NMOS transistor is I, the charge CV is extracted as from the rising of the clock Q(n-1)1 during the time tCKn with the constant current I, while being extracted during the remaining period with the constant current 2I. As a result, the time

$$tCKn+(CV-tCKn \cdot I)/2I$$
$$=CV/2I+tCKn/2 \qquad \cdots(2)$$

represents the timing difference from the rising edge of the clock Q(n-1)1 to the rising edge of the clock T22.

[0046]

That is, the timing difference between the rising of the clock T22 and the rising of the clock T21 is tCKn/2.

[0047]

When the clocks Q(n-1)1 and Q(n-1)2 both go to a low level, and the node N1 is charged through the P-channel MOS transistor MP01 from the power supply to a high level, the clock T22 falls. The same applies for the clocks T22 to T28, and the timing difference of the clocks T21 to T28 is equal to tCKn/2.

[0048]

The pulse correction circuits 216 to 223 generate duty-25% eight-phase pulses P21 to P28, each phase of which is shifted by 45° from one another (see Figs.9 and 10).

[0049]

The multiplexer circuits 224 to 227 generate duty 50% four-phase pulses Qn1 to Qn4, each phase of which is shifted by 90° from one another(see Figs.9 and 10).

[0050]

The timing difference division circuit shown in Fig.12 is suitably changed depending on the application used. For example, it is possible to provide an output signal of a NAND circuit which receives the first and second input signals IN1 and IN2, to the gate of the P-channel MOS transistor MP01 and to provide the signals which are obtained on complementing the first input signal IN1 and the second input signal IN2 by the inverter, to the gates of the N-channel MOS transistors MN01 and MN02. In this case, when the first and second input signals IN1 and IN2 are at a high level, the P-channel MOS transistor MP01 is turned on to charge the internal node N1, with the output of the inverter INV01 going to a low level. When one or both of the first and second input signals IN1 and IN2 are at a low level, the P-channel MOS transistor MP01 is turned off, and one or both of the P-channel MOS transistors MN01 and MN02 is turned on to discharge the internal node N1. When the voltage of the internal node N1 falls to below the threshold value of the inverter INV01, the output of the inverter INV01 rises to a high level.

[0051]

The meritorious effects of the present invention are summarized as follows.

According to the present invention, as described above, the frequency range can be modified readily to facilitate adjustment of

characteristic values. The reason is that in accordance with the present invention, changes in the frequency can be coped with by varying the value of the capacitance added to the internal node of the interpolator forming a phase shift circuit designed for shifting the phase of the multi-phase clocks and for outputting the so phase-shifted clocks.

[0052]

Moreover, according to the present invention, in which the selection circuit is provided, there may be derived an advantage that it is possible to variably set the parallel number in the clock and data recovery circuit.

It should be noted that other objects, features and aspects of the present invention will become apparent in the entire disclosure and that modifications may be done without departing the gist and scope of the present invention as disclosed herein and claimed as appended herewith.

Also it should be noted that any combination of the disclosed and/or claimed elements, matters and/or items might fall under the modifications aforementioned.